

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D. RemarksRejections Under 35 U.S.C. §112, Second Paragraph.

5           Claims 33, 41, and 53 have been amended to address these rejections. Claims 41 and 53 have been amended as suggested by the examiner.

Non-statutory Obvious-Type Double Patenting Rejection of Claims 33-53 based on Walker (U.S. Patent No. 6,064,589).

10           The invention of amended claim 33 includes a random access memory cell. The random access memory cell includes a pass transistor is coupled to a data storage node to provide charge transfer to and from the data storage node. The pass transistor includes a source region, a drain region, and a channel region. The channel region includes a first channel side and a second channel side opposite to the first channel side. The pass transistor further includes a first channel  
15           side control gate and a second channel side control gate. The first channel side control gate is formed in a trench.

          As is well established, analysis for an obvious-type double patenting rejection should make clear (1) the differences between the inventions defined by the conflicting claims; and (2) the reasons why the invention is an obvious variation of the invention defined in a claim of the patent.<sup>1</sup> The burden to make such a showing rests on the Examiner. Further, the showing of  
20           obviousness must follow the analysis used to establish a prima facie case of obviousness.<sup>2</sup>

          The above noted requirement is repeated in the MPEP, as shown below:

          Any obviousness-type double patenting rejection should make clear:

25           (A) The differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application; and

          (B) The **reasons why** a person of ordinary skill in the art would conclude that the invention defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent.

          (MPEP §804(II)(B)(1), emphasis added).

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          The standard rejection language provided by the MPEP also indicates that some sort of rationale is required to meet the burden:

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<sup>1</sup> See MPEP §804(II)(B)(1).

¶ 8.34 Rejection, Obviousness Type Double Patenting - No Secondary Reference(s)

Claim [1] rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim [2] of U.S. Patent No. [3]. Although the conflicting claims are not identical, they are not patentable distinct from each other because [4].

Examiner Note...

8. In **bracket 4**, **provide appropriate rationale of obviousness** for any claims being rejected over the claims of the cited patent.

(MPEP §804(II)(B)(1), emphasis added).

The present rejection only provides a conclusion of obviousness.<sup>3</sup> Consequently, the necessary burden to show why the present claims are obvious in light of *Walker* cannot have been met.

For this reason alone, this ground for rejection is traversed.

In addition or alternatively, as is well known, the requirements for a prima facie case of obviousness (which a non-statutory double-patenting rejection must meet) include (1) some suggestion or motivation to modify a reference or combine reference teachings; (2) a reasonable expectation of success; and (3) the prior art reference(s) must teach or suggest all claim limitations.

While Applicant strongly believes that the above-rationale cannot have shifted the burden of proof from the Examiner to Applicant, Applicant nevertheless notes that amended claim 33 includes clear limitations that are shown in claims 1-4, 7, 10-12, 15, and 17 of *Walker*. In particular, and as but one particular example, amended claim 33 recites that the first channel side control gate is formed in a trench. Such a feature is not believed to be explicitly shown in any of claims 1-4, 7, 10-12, 15, and 17 of *Walker*.

<sup>2</sup> *In re Longi*, 759 F.2d 887 (Fed Cir. 1985).

<sup>3</sup> See the Office Action, dated 11/16/2004, Page 2, third full paragraph. The rationale only states that the claims are "drawn to substantially the same random access memory having a double-gate access transistor coupled to a storage capacitor". This is not a rationale, but rather a conclusion.

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Accordingly, all the limitations of the claims are not believed to be shown or suggested, and a prima facie case of non-statutory double patenting is not believed to exist.

Claims 33, 41, and 53 have been amended not in response to the cited art, but to address  
5 typographical errors.

The present claims 33-53 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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 1/13/05  
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